Ayushi Agarwal

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Indian Institute of Technology Delhi

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Ph.D.

Examination	Institute	Year	CPI/%
Ph.D.	IIT Delhi	Ongoing	9.62
B.Tech. (ECE)	NIT Allahabad	2010-14	9.65 (**Rank 1**)
Intermediate/+2	CMS, Lucknow	2007-09	97.5 (**Rank 2**)
Matriculation	CMS, Lucknow	2006	96.2

ACADEMIC/PROFESSIONAL ACHIEVEMENTS

- **Prime Minister Research Fellowship (PMRF)**, May 2020 cycle
- First prize in **Cadence Tensilica Hackathon** at VLSI Design Conference 2019
- **Six Qualcomm Star Employee Awards**, Qualcomm BDC, 2014-2017
- **LATE (DR.) MALAY RAJ MUKHERJEE GOLD MEDAL** for standing first amongst the students of B.Tech. (Electrical Engineering), B.Tech. (Electronics and Communication Engineering) and B.Tech. (Computer Science and Engineering) Examination, 2014
- **Institute GOLD MEDAL for being the Institute topper** in Electronics and Communication Engineering,2014
- **OP Jindal Engineering & Management Scholarship, 2012** awarded by Jindal Steel & Power Limited for exhibiting outstanding competency, leadership and personality traits
- **Science Honour and Cash Prize**, Dept. of Science and Technology, Uttar Pradesh, 2009

WORK EXPERIENCE & INTERNSHIPS

- **PhD Research Scholar** | ***MARG, Indian Institute of Technology Delhi*** *(July'19-present)*
  - Research Interests: Computer Architecture, System-on-Chip, AI Accelerators
  - Hardware for Machine learning on Edge-devices
  - Design and System-level integration of Machine Learning Accelerators on Multi-processor SoCs
- **Technical Intern** | ***NXP Semiconductors, Bangalore*** *(March'21-July'21)*
  - Memory tracing on AI/ML applications on LX2160A and S32G2 NXP SoCs
- **Project Engineer** | ***MARG, Indian Institute of Technology Delhi*** *(July'18-Dec'18)*
  - Data Analysis for Cache-Bandwidth Partitioning Algorithms at LLC
  - Cache Bandwidth Allocation Management in multi-core processors
- **Research Engineer** | ***GreenIC, National University of Singapore*** *(July'17-June'18)*
  - Algorithm Design for Energy-Efficient Hardware Acceleration of Neural Networks on Custom Accelerators
  - Design of re-configurable hardware accelerators for Deep Learning Applications
- **Digital Design Engineer** | ***Qualcomm, Bangalore Design Center*** *(July'14-June'17)*
  - Designed the NoC (Network on Chip) for MDM 9x55 and 9x75 and Snapdragon 820, 835 and other SoCs
  - Led TLM performance Analysis for all the SoC Interconnects
  - Led PPA (Power, Performance and Area) analysis for wearable chips of Qualcomm
  - Awarded 6 Qualstars awards for solving critical issues, team spirit and contributing significantly to projects
- **Interim Engineering Intern** | ***Qualcomm, Bangalore Design Center*** *(May'13-July'13)*
  - Automatic validation of SoC Bus RTL and Performance Analysis of SoC Bus System using PERL
- **Design Intern** | ***CETPA Infotech Pvt. Ltd.*** *(May'12-June'12)*
  - 16- bit Microprocessor RTL design and implementation on FPGA

TECHNICAL SKILLS

- **Machine Learning**: Good understanding of Convolutional Neural Networks
- **VLSI**: RTL Design, Bus protocols, System Architecture Design, RTL for full tile silicon flow, RTL Synthesis and Timing Analysis, Performance Bottleneck Analysis, TLM performance flow
- **Programming & Scripting Languages**: VHDL, Verilog, Python, C, C++, HTML, Shell, Perl
- **Tools & Libraries**: MATLAB, LaTeX, OpenCV, Gem5 Simulator, Snipersim, CAFFE, TensorFlow, ModelSim, VCS, Synopsys Design Compiler, FlexNoC, Spyglass, 0in, Proteus ISIS, Xilinx ISE

COURSES & PROJECTS

- **Memory-Constrained Analysis of CNN Training**, *(COL861 - Special Topics in Hardware Systems)* *(Aug'20-Jan'21)*
  - Theoretical Analysis of CNN training to understand compute and memory requirements for different phases of training
  - Accelerator Architecture proposal based on the observations from the analysis
- **Image Stitching on FPGA**, *(COL812 - System-Level Design and Modeling)* *(Jan'20-Aug'20)*
  - Application profiling to divide the workload between software and hardware
  - Implementation of hardware part on FPGA using Vivado
- **Image-Captioning Machine Learning Model**, *(COL774 - Machine Learning)* *(Jan'20-Aug'20)*
  - Generate captions for images using a machine learning model trained in PyTorch
  - Designed a CNN based encoder to encode the image features
  - Designed a LSTM/Attention based decoder to generate captions from CNN features
- **Parallel Edit Distance**, *(COL730 - Parallel Programming)* *(July'19-Nov'19)*
  - Implementation of algorithm to calculate edit distance between two strings using parallel programming languages like OpenMP and MPI
- **System Analysis of High-Performance Computers**, *(COL718 - Arch. of High-Performance Computers)* *(July'19 - Nov'19)*
  - Created micro-benchmarks to study the the architecture (ROB size, PRF, MLP and Memory hierarchy parameters) of high-performance computers
  - Analysis of performance of SPEC 2017 benchmarks on different type of cores including SMT, SMP and CMP
- **Embedded Systems**
  - Heart rate counter using 8051 micro-controllers *(Final Year Project at NIT, Allahabad)*
  - OFDM hardware implementation *(Final Year Project at NIT, Allahabad)*
  - 16-bit Microprocessor Design and implementation on FPGA *(Project at CETPA Infotech Lab)*

POR & EXTRA-CURRICULARS

- **Teaching Assistant** for the course, **COL215 : Digital Logic and System Design**, supervised the labs for the course, evaluated their lab assignments, quizzes and examination papers *(Aug'20-Jan'21 & July'21-Present)*
- **Teaching Assistant** for the course, **COL216 : Computer Architecture**, supervised the labs for the course, designed and evaluated their lab assignments, quizzes and examination papers *(Jan'20-July'20)*
- **Teaching Assistant** for the course, **COL719 : Synthesis of Digital Systems**, supervised the labs for the course, designed and evaluated their lab assignments, quizzes and examination papers *(July'19-Dec'19)*
- **Volunteer** for She Codes Foundation *(Jan'20-ongoing)*
- **Vice-Chairperson**, IEEE MNNIT Student Chapter *(July'13 - June'14)*
- **Hackathon Organizer** from i3indya technologies on Cyber solutions and CETPA Infotech workshop on microprocessor design *(July'13 - June'14)*
- **Festival Secretary** for cultural festival **CULRAV'14** at MNNIT, Allahabad *(Jan'14 - April'14)*
- **Festival Secretary** for technical festival **AVISHKAR'13** at MNNIT, Allahabad *(July'13 - Dec'13)*
- **OPJEMS Scholar** for leadership skills and problem-solving capabilities. *(August 2012)*